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Description

Testing of Mixed Signal Integrated Circuits Generating Analog Signals From Digital Data Elements

BACKGROUND OF INVENTION

[0001] *Field of the Invention*

[0002] The present invention relates to testing of integrated circuits, and more specifically to a method and apparatus for testing mixed signal integrated circuits which generate analog signals from digital data elements.

[0003] *Related Art*

[0004] Mixed signal integrated circuits (IC) generally refer to circuits which operate on both analog and digital signals. Mixed signal ICs are used in several areas such as communications (both wireless and wire-based) in which digital data elements are converted into analog signals which are eventually transmitted.

[0005] A receiving system (using another mixed signal IC) recov-

ers the digital data elements from the analog signals. Other digital data elements may then be transferred in the reverse direction as well. The data thus exchanged is used to support several user applications (e.g., voice calls, networking), as is well known in the relevant arts.

[0006] Testing is often performed to determine whether an integrated circuit operates according to design specifications. It may be necessary to discard at least integrated circuits which substantially deviate from the design specification. Thus, by performing such testing, one may ensure that only end products which provide an intended utility, are supplied/sold in the market place.

[0007] It is often desirable to test an IC before the IC is integrated into end products, which are eventually sold/supplied. As an illustration, an IC may be placed in a package, the packaged IC may then be placed on a board, and the board may be eventually used in a system which is sold/supplied to an end customer. By testing and discarding the IC at an early stage (e.g., before being placed in a package), unneeded wastage of resources (cost/time/effort) may be avoided.

[0008] In one prior testing approach, a transceiver (containing a transmitter, receiver and an antenna) is placed in a loop-

back mode in which the output of the transmitter is connected to the input of the receiver, bypassing the antenna. The transmitter converts a sequence of digital data elements into analog signals, which are received by the receiver. The receiver generates a sequence of digital data elements from the received analog signal. Deviations from the design specifications may be determined based on the signal strength of the received analog signals, comparison of the digital data elements used in the transmitter and receiver, etc.

[0009] Thus, the prior approach of above enables testing of a transceiver, potentially when the corresponding IC is not yet packaged (and thus only as a stand-alone wafer). one problem with the approach is that many transceivers use common components in the transmit and receive paths, and simultaneous use of both the paths may not thus be possible. In addition, loopback approaches often skip some portions/stages of the transmit/receive paths, and the test results may accordingly not be reliable.

[0010] What is therefore needed is an improved method and apparatus for testing of mixed signal integrated circuits generating analog signals from digital data elements.

Brief Description of Drawings

[0011] The present invention will be described with reference to the following accompanying drawings.

[0012] Figure 1is a block diagram illustrating an example environment in which the present invention may be implemented.

[0013] Figure 2 is a flow-chart illustrating the details of a method using which testing of an IC may be performed according to an aspect of present invention.

[0014] Figure 3 is a block diagram illustrating the details of testing a transceiver according to an aspect of the present invention.

[0015] Figure 4 is a constellation diagram illustrating the manner in which error vector magnitude may be measured, which in turn is used to determine whether to discard/qualify a mixed signal IC.

[0016] Figure 5 is a block diagram illustrating an example device in which various aspects of the present invention can be implemented.

[0017] In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.

DETAILED DESCRIPTION

[0018] *1. Overview*

[0019] An aspect of the present invention enables testing of a mixed signal integrated circuit (IC) by employing a calibrated (tested) integrated circuit. To test a mixed signal IC in the transmit direction, a symbol (digital data element) is converted into an analog signal at the mixed signal IC. The analog signal is transmitted to a calibrated integrated circuit. The calibrated integrated circuit determines a valid symbol corresponding to the signal level on the received analog signal.

[0020] An error magnitude may be measured based on the deviation of the signal level of the received analog signal from a signal level corresponding to the determined valid symbols. The deviation of the mixed signal IC from design specification may be ascertained by performing such measurements corresponding to several symbols. The mixed signal IC may be discarded if the deviation is above a pre-specified threshold. Thus, as aspect of the present invention enables a mixed signal IC to be tested.

[0021] According to another aspect of the present invention, the approach described above is implemented with the mixed

signal IC being present in the form of a stand-alone die (i.e., not placed in a package). The calibrated IC also can be used in the form of a stand-along die. As a result, unneeded wastage of resources (cost/time/effort with respect to defective ICs) may be avoided. The cost of testing can be further reduced bycircuit portions generating the symbols and measurement of the error magnitude within the same die as the mixed signal IC.

[0022] Several aspects of the invention are described below with reference to examples for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide a full understanding of the invention. One skilled in the relevant art, however, will readily recognize that the invention can be practiced without one or more of the specific details, or with other methods, etc. In other instances, well_known structures or operations are not shown in detail to avoid obscuring the invention.

[0023] *2. Example Environment*

[0024] Figure 1 is a block diagram illustrating an example environment in which various aspects of the present invention may be implemented. The block diagram is shown containing symbol generator 110, mixed signal IC 130, probe

pad 140, calibrated IC 150, and tester 180. Each block is described below in detail.

[0025] Symbol generator 110 generates a sequence of symbols used for testing mixed signal IC 130. As described below, the symbols can be used to test both the receive and the transmit paths of mixed signal IC 130. In an embodiment, each symbol contains two vector (I and Q) components, each being referred to as a digital data element.

[0026] Probe pad 140 enables the electrical connection of appropriate signal leads of the two ICs 130 and 150. For example, the transmit path of one IC may be connected to the receive path of the other IC. The connections thus provided enable mixed signal IC 130 to be tested without being packaged, thereby avoiding unneeded wastage of resources with respect to ICs that are eventually discarded. Probe pad 140 can be implemented using one of several commercially available products.

[0027] Mixed signal IC 130 represents an example IC which can be tested using various aspects of the present invention. Calibrated IC 150 represents an IC which is already tested and/or calibrated such that the operation of the IC can be assumed to be accurate while performing tests.

[0028] Tester 180 tests mixed signal IC 130 according to various

aspects of the present invention. Tester 180 may receive from symbol generator 110 the data inputs (symbols/vectors) used for such testing. In an embodiment, the entire transmit and receive paths are tested. The manner in which mixed signal IC 130 can be tested in such an environment is described below with additional examples.

[0029] *3. Method*

[0030] Figure 2 is a flow-chart illustrating the details of a method using which a mixed signal IC may be tested according to an aspect of present invention. The method is described with reference to Figure 1 for illustration. However, various aspects of the present invention can be implemented in other environments as well, as will be apparent to one skilled in the relevant arts by reading the disclosure provided herein.

[0031] For illustration, it is assumed that mixed signal IC 130 is operating in transmit-mode and calibrated IC 150 is operating in receive-mode. However, similar approach may be used to test mixed signal IC 130 in the reverse direction (i.e., mixed signal IC 130 receiving from calibrated IC 150). The method begins in step 201 in which the control immediately passes to step 210.

[0032] In step 210, mixed signal IC 130 converts a sequence of

symbols to a corresponding analog signal. Thus, a portion of the analog signal may be generated from a corresponding symbol. symbols may be provided to mixed signal IC 130 by symbol generator 110.

[0033] In step 220, mixed signal IC 130 transmits the analog signal to calibrated IC 150. The analog signal may be transmitted to calibrated IC 150 via probe pad 140. In step 230, the analog signal is received by calibrated IC 150.

[0034] In step 250, calibrated IC 150 determines valid symbols corresponding to the portions of received analog signal. For example, the voltage level of a portion of the received analog signal may be examined to determine the closest voltage level associated with one of the valid symbols. Such a symbol may be deemed to be the valid symbol for the corresponding analog signal portion. An example approach to determine valid symbols in case a symbol contains multiple vector components, is described below in further detail.

[0035] In step 270, calibrated IC 150 measures the deviation of the signal level of the received analog signal from the signal level corresponding to the determined valid symbols. One of various known approaches may be used for such measurement depending on the manner in which the

symbols are represented, etc. In an embodiment described below, the deviation of may be measured according to IEEE 802.11a protocol standard well known in the relevant arts.

[0036] In step 280, a value representing the deviation to is sent to tester 180, which compares the received value with a pre-specified threshold value. Mixed signal IC 130 may be determined to be acceptable (qualified) if the value is less than the threshold value, and may be discarded otherwise. The method ends in step 299.

[0037] As the IC (i.e., calibrated IC 150) at the other end is calibrated, the deviation from the determined valid symbols generally represents the error introduced by the IC sought to be tested. Accordingly, a measure of the deviations can be used to qualify or discard an IC. The description is continued with respect to example embodiment(s) implementing various features described above.

[0038] *4. Testing a Mixed Signal Integrated Circuit*

[0039] Figure 3 is a block diagram illustrating the details of testing a mixed signal integrated circuit according to an aspect of the present invention. The block diagram is shown containing details of transmitter 330 (e.g., contained in mixed signal IC 130) and receiver 380 (e.g., contained in

calibrated IC 150) assumed to be contained in different ICs. However, it should be appreciated that typical ICs contain both transmitter and receiver. Each block of Figure 3 is described below in further detail.

[0040] Transmitter 330 (contained in mixed signal IC 130) is shown containing digital to analog converters (DAC) 331 and 332, up_conversion mixers 334and 336, and adder 337. DACs 331 and 332 respectively generate a corresponding baseband signal by converting a component (I and Q respectively) of an input symbol received on path 113. Each pair of corresponding I and Q components forms a transmitted symbol. The resulting baseband signals are provided as inputs to up-conversion mixers 334 and 336.

[0041] It should be understood that the path from DAC 331 to mixer 334 may contain several components such as filters and amplifiers (which may together be referred to as an analog front end). Similar components may also be present in the path from DAC 332 to mixer 336, mixer 384 to ADC 381, and mixer 388 and ADC 382. Such components are not shown merely to avoid obscuring various aspects of the present invention. However, various aspects of the present invention ensure that all such intermediate

components in both the transmit and receive paths are tested.

[0042] A common carrier signal is shown received from local oscillator 389 (contained in receiver 380), and accordingly a separate local oscillator is not shown to be present in transmitter 330. By using a common carrier signal, various challenges related to synchronization may be avoided during testing. However, transmitter 330 contains a local oscillator implemented to operate in a manner similar to that of local oscillator 389 described below. Phase shifter 333 shifts an input signal (received from oscillator 389) by 90 degrees, and the shifted signal is provided as a carrier signal to up-conversion mixer 334.

[0043] Up-conversion mixer 334 modulates the carrier signal using the baseband signal (encoding the sequence of vector components) received from DAC 331, and generates a modulated carrier signal component. Similarly, up-conversion mixer 336 also generates another modulated carrier signal component by modulating the corresponding carrier signal. Due to the operation of phase shifter 333, the two carrier signals are out-of-phase by 90 degrees. Adder 337 logically represents the addition of the two modulated carrier signal components, and the result-

ing analog signal is provided on path 370.

[0044] Receiver 380 is shown containing analog-to-digital convertors (ADC) 381 and 382, down_conversion mixers 384 and 388, and local oscillator 389. Local oscillator 389 generates a carrier signal, which is phase-shifted by 90 degrees by phase shifter 383. The two signals (out-of-phase by 90 degrees) are provided as respective carrier signals to down-conversion mixers 384 and 388. As noted above, local oscillator 389 may provide the carrier signals for transmitter 330 as well.

[0045] Down_conversion mixer 384 de_modulates one of the two (here the output generated by up-conversion mixer 336) out-of-phase components present in the analog signal received on path 370 using the carrier signal received from oscillator 389 to generate a corresponding baseband signal. Similarly, down conversion mixer 388 demodulates the other phase component of the received analog signal using the carrier signal received from phase shifter 383, and provides the resulting baseband signal to ADC 382.

[0046] ADC 381 generates a sequence of I-vector components by sampling the baseband signal received from down-conversion mixer 384. ADC 382 generates a sequence of

Q-vector components by sampling the baseband signal received from down-conversion mixer 388. It may be appreciated each pair of corresponding I and Q vector components together form a received vector combination.

[0047] EVM computation block 390 computes a error vector magnitude (EVM) based on the received vector combinations from the corresponding valid symbols. The EVM is provided as an input to tester 180, which determines whether to qualify/discard mixed signal IC 130. EVM computation block 390 may be implemented within or external to mixed signal IC 130. The operation of an embodiment of EVM computation block 390 is described below in further detail.

[0048] *5. Error Vector Magnitude (EVM)*

[0049] Figure 4 is a constellation diagram illustrating the manner in which the deviation of received vector combinations from corresponding valid symbols may be measured in one embodiment. As noted above, the deviation is used to discard/qualify an integrated circuit. The constellation diagram is shown containing values for I and Q vector components along x-axis and y-axis respectively. Sixteen points ((4,4) (4,8), ... (16,16)) represent the corresponding sixteen valid symbols V11 through V44.

[0050] For illustration, it is assumed that ADC 381 generates a sequence of vector components (for I vector) equaling (5, 7, and 14), and ADC 382 generates the corresponding values of Q vector equaling (15, 5, and 9). As may be appreciated, the generated component values represent the voltage levels of the respective portion of the analog baseband signal sampled by the ADC. Thus, three received vector combinations equaling A1 (5, 15), A2 (7, 5), and A3(14, 9) are provided to EVM computation block 390, which generates the EVM value.

[0051] EVM computation block 390 may then determine the valid symbols corresponding to the received vector combinations. In one embodiment, the component values representing the transmitted symbols (provided to DACs 331 and 332) are also provided to EVM computation block 390 (connection to EVM computation block 390 not shown). Thus, such provided values are used to compute the EVM.

[0052] In an alternative embodiment, each component of the received vector combination is mapped to a corresponding closest valid component. The valid components then form the valid symbol corresponding to the received vector combination. For example, with respect to A1 (5, 15), the value 5 may be mapped to 4, and the value 15 is mapped

to 16, thereby determining the corresponding valid symbol to equal (4, 16). Similarly, (8, 4) and (16, 8) are respectively determined to be the corresponding valid symbols for A2 (7, 5) and A3 (14, 9).

[0053] The deviation of each received vector combination from a corresponding valid symbol may be measured by the geometric distance between the two symbols. EVM may be computed as equal to root-mean-square (RMS) average of deviations for a sequence of received vector combinations. In the illustrative example, EVM is computed as equal to square root of $\{((5-4)^2+(15-16)^2)+((7-8)^2+(5-4)^2)+((14-16)^2+(9-8)^2)\}= 3$. Alternatively, EVM may be measured by the RMS average of all errors in a packet (or sequence of symbols)as specified by 802.11a wireless standard, well known in the relevant arts.

[0054] Mixed signal IC 130 may then be either discarded or qualified based on the EVM value thus generated. The mixed signal ICs thus tested can be placed in various devices. An example device is described briefly below.

[0055] *6. Example Device*

[0056] Figure 5 is a block diagram illustrating an example device in which various aspects of the present invention can be implemented. Device 500 is shown containing processing

block 510 and transceiver 530.530 may be implemented using receiver 380 and transmitter 330 described above. Transceiver 530 is used to send symbols generated by processing block 510 in the form of analog signals using antenna 535.transceiver 530 is used to receive analog signals, and provide the corresponding symbols (or equivalent bit stream) to processing block 510.

[0057] Processing block 510 implements various applications (such as converting the data to audible voice in the case of a mobile phone, data networking applications, etc.) using the data stream contained in the symbols.

[0058] *7. Conclusion*

[0059] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.